Online Junction-Temperature Sensing of SiC MOSFETs with Minimal Calibration Effort

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Abstract

This work proposes a junction-temperature sensing method for silicon-carbide (SiC) MOSFETs with minimal calibration effort. The method utilizes the time delay between the gate-voltage and the device-current rise as a temperature-sensitive electrical parameter (TSEP) that exhibits two unique features: The time delay depends linearly on the junction temperature and shows nearly no sensitivity to the device current. Both features combined yield junction-temperature sensing with minimized calibration effort that is crucial for practical applications. Furthermore, this work demonstrates that the specific temperature dependence of the charge carrier mobility of SiC devices renders the sensing method particularly suitable for the application on SiC MOSFETs. This paper first defines the considered TSEP and describes the corresponding junction-temperature sensing method. Subsequently, a sensitivity analysis is performed to identify the influences on the considered time delay and to analyze the differences in the behavior of the TSEP for Si and SiC devices. Lastly, the method is validated by measurements on an SiC power module.

1 Introduction

Power electronic systems are increasingly used in applications where an unforeseen critical failure can lead to economic damage or even worse, personal injury. Examples of such applications are electric vehicles [1], [2], trains [3] and aircrafts [4] as well as energy supply systems. The utilization of power-electronic systems in such mission-critical components results in higher reliability requirements.

Thermomechanical fatigue induced by thermal cycles during operation is a root cause for the degradation of power-electronic modules [5]–[8]. This is especially the case for SiC power modules in highly integrated applications [9]–[11] as they are particularly affected by degradation through thermal cycling due to their smaller footprint and lower thermal capacity in comparison to Si devices [12]. Therefore, condition monitoring is a key technology for increasing reliability of SiC power modules by determining component condition [13]–[15] and predicting lifetime [16]. Promising approaches using 3-D thermal models and observer control structures have shown that thermal cycles in power modules can be determined with high accuracy [13], [17] and even mitigated via active thermal control [18]. However, these methods depend on high-bandwidth junction-temperature measurements of the power devices. Currently, temperature measurement in power modules is most commonly realized by using negative temperature coefficient (NTC) thermistors [19]. Although temperature information is easily extracted, thermistors are usually not placed in close proximity to the switching power components preventing high-bandwidth measurements. As an alternative, the extraction of temperature-sensitive electrical parameters (TSEPs) represents a promising sensing approach [20]–[22]. These parameters are usually directly dependent on the power-device junction temperature which enables high bandwidth measurement. For temperature extraction, sensing circuits are used that are directly connected to the power-module terminals. TSEPs for SiC MOSFETs that have already been investigated include the on-state voltage [20], the turn-off delay time [23] as well as the device current rate of change [24]. These TSEPs all share the common characteristic that they are both junction-temperature and device-current dependent. This significantly increases the calibration effort since a 3-D look-up table for the junction temperature depending on the TSEP value as well as the device current must be generated. Additionally, a corresponding measured current value must be available at the time of the temperature extraction.

This work aims to overcome this limitation by utilizing the turn-on time delay between the rise of the gate voltage and the rise of the device current as a TSEP. This parameter linearly depends on the junction temperature and shows nearly no sensitivity to the device current. This allows calibration with minimal effort as only two measuring points are required. While the basic functionality of this TSEP was demonstrated for Si devices in previous research [25], this paper identifies the fundamentally different temperature dependency of the charge carrier mobility of SiC compared to Si devices as a key enabling factor that makes the method particularly attractive for the use in SiC MOSFETs.

First, the work defines the considered TSEP and describes how the parameter can be extracted with the proposed junction-temperature sensing method. Subsequently, a sensitivity analysis is performed to determine which component-specific quantities influence the temperature dependency of the TSEP. The difference in sensitivity between Si and SiC devices is discussed and it is shown why the method is especially suitable for the application on SiC MOSFETs. Finally, the described properties are validated by measurements on an SiC power module using a double-pulse test bench with temperature control unit.
2 Temperature Sensing Method

The considered junction-temperature sensing method utilizes the parasitic inductance \( L_{SS} \) between the kelvin-source (S’S) and power-source (S) terminals of a SiC MOSFET, which can be seen in Fig. 1. The voltage across this inductance \( u_{SS} \) is directly dependent on the device current rate of change \( \frac{di_{DS}}{dt} \) according to

\[
u_{SS} = L_{SS} \cdot \frac{di_{DS}}{dt}.
\] (1)

The TSEP that is used for this sensing method is the turn-on time delay. It starts with the rising edge of the gate voltage \( U_{GS,m} \) and ends when a pre-defined voltage level \( U_{SS,lev} \) of the parasitic inductance voltage \( u_{SS} \) is reached. The overall time delay \( t_{02} \) is divided into two time periods \( t_{01} \) and \( t_{12} \), which are shown in Fig. 2.

During the first period \( t_{01} \), i.e., between the rising edge of the driver voltage \( U_D \) and the time instant at which the gate voltage \( U_{GS,m} \) reaches the threshold voltage \( U_{th} \), no device current is flowing. During this period, the time-dependent gate voltage can be determined by

\[
u_{GS,m} = U_{D,off} + (U_{D,on} - U_{D,off}) \cdot \left(1 - e^{-\frac{t_{01}}{\tau}}\right),
\] (2)

whereby \( U_{D,off} \) is the low-level and \( U_{D,on} \) the high-level driver voltage. The gate charge time constant \( \tau \) can be calculated using the combined external and internal gate resistance \( R_G(T) = R_{G,ext}(T) + R_{G,int}(T) \) and the parasitic input capacitance \( C_{iss} = C_{GS} + C_{GD} \) by

\[\tau = R_G(T) \cdot C_{iss}.\]

With equation (2) and the conditions \( t_0 = 0 \) s and \( u_{GS,m}(t_1) = U_{th}(T) \), the time period \( t_{01} \) can be determined as follows:

\[t_{01}(T) = -R_G(T) \cdot C_{iss} \cdot \ln \left(\frac{U_{D,on} - U_{th}(T)}{U_{D,on} - U_{D,off}}\right).
\] (3)

Equation (3) shows that the first time period is influenced by junction temperature due to the temperature sensitivity of the gate resistance \( R_G \) and the threshold voltage \( U_{th} \). The temperature sensitivity of the gate resistance is influenced by both the external and internal gate resistance. However, the influence of the external gate resistance can be neglected if the gate driver is thermally weakly connected to the power module and the self-heating is minor. The input device capacitance \( C_{iss} \) [26] as well as the driver voltages can be considered temperature independent.

The second time period \( t_{12} \) starts with the device-current rise at \( t = t_1 \) and ends when the voltage \( u_{SS} \) across the parasitic inductance \( L_{SS} \) reaches the pre-defined level \( U_{SS,lev} \). Since the device operates in its saturation region, the n-type MOSFET behavior can be described using the transconductance gain \( K_n \) by

\[i_{DS} = \frac{1}{2} \cdot K_n(T) \cdot (u_{GS,m} - U_{th}(T))^2.
\] (4)

The transconductance gain \( K_n \) is defined as

\[K_n(T) = \mu_n(T) \cdot C_{ox} \cdot \frac{W}{L},
\] (5)

whereby \( \mu_n \) is the charge carrier mobility, \( C_{ox} \) the surface-specific gate capacitance and \( W \) and \( L \) the width and length of the gate, respectively. By combining equations (1), (2) and (4) as well as the condition \( u_{SS}(t_{12}) = U_{SS,lev} \), the second time period \( t_{12} \) can be condensed to

\[t_{12}(T) = -R_G(T) \cdot C_{iss} \cdot \ln \left(\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{R_G(T) \cdot C_{iss} \cdot U_{SS,lev}}{L_{SS} \cdot K_n(T) \cdot (U_{D,on} - U_{th}(T))^2}}\right).
\] (6)

Equation (6) shows that the second time period is influenced by junction temperature due to the gate resistance \( R_G \), the threshold voltage \( U_{th} \) and the transconductance gain \( K_n \). The temperature dependency of the gain \( K_n \) is mainly caused by the carrier mobility \( \mu_n \), which can be seen in equation (5). Like capacitance \( C_{iss} \), the inductance \( L_{SS} \) can be assumed to be temperature insensitive [26].

The total delay \( t_{02} \) corresponding to the considered TSEP is defined as

\[t_{02}(T) = t_{01}(T) + t_{12}(T).
\]
The fact that the time periods in equations (3) and (6) do not depend on the device current $i_D$, enables a current-independent calibration of the considered TSEP and implies that no current measurement value needs to be provided during operation. This reduces the calibration effort for online temperature measurements significantly.

### 3 Sensitivity Analysis

In order to evaluate the overall junction-temperature sensitivity of the considered TSEP, the sensitivities of the individual components of the time periods in equations (3) and (6) need to be examined. As discussed in the proceeding section, the gate resistance $R_G$, the threshold voltage $U_{th}$, and the transconductance gain $K_n$ are the main influences on the temperature sensitivity of the TSEP, while the driver voltages $U_{D,\text{on}}$ and $U_{D,\text{off}}$ as well as the parasitic inductance $L_{\text{S,S}}$ and capacitance $C_{\text{iss}}$ are considered temperature independent. In the following, the three main influences on the temperature sensitivity of the TSEP are individually discussed.

#### 3.1 Gate Resistance $R_G$

The total gate resistance $R_G$ is the combination of the external $R_{\text{G,ext}}$ and internal $R_{\text{G,int}}$ gate resistance. While the internal gate resistor is an intrinsic part of the transistor, the external resistor is part of the driver circuit connected to the power module. Due to the location of the internal gate resistance, there is a direct relationship between the temperature-related change in resistance and the junction temperature of the transistor. On the other hand, the external resistor is in most cases thermally not well connected to the transistor. It follows that the resistance value of the external resistor is mainly influenced by its self-heating due to losses and fluctuations of the ambient temperature. Because of this and due to the fact that the temperature coefficient of the external gate resistance ($10 \text{ ppm} \ldots 100 \text{ ppm}$) is usually much smaller than of the internal gate resistance [21], [27], the influence of the external gate resistance on the considered TSEP can be neglected.

As can be seen in equations (3) and (6), both the time periods $t_{01}$ and $t_{12}$ lengthen with an increasing value of the gate resistance $R_G$. Since the internal gate resistance has a positive temperature coefficient, it has a prolonging influence on the turn-on delay with increasing temperature.

#### 3.2 Threshold Voltage $U_{th}$

The threshold voltage $U_{th}$ is the minimum gate-source voltage $U_{GS}$ required to allow a current flow in the transistor. Since the bandgap decreases and the carrier concentration increases for higher temperatures, the threshold voltage decreases with rising junction temperatures [28]. Thus, the threshold voltage has a negative temperature coefficient. With regard to equations (3) and (6), the negative temperature coefficient of the threshold voltage has a shortening influence on both time periods $t_{01}$ and $t_{12}$ with rising temperature.

#### 3.3 Transconductance Gain $K_n$

The transconductance gain $K_n$ is a characteristic parameter of MOSFETs and is used to describe the device behavior during switching. The parameter is employed to determine the device current $i_D$ during the saturation region, as shown in equation (4), and the linear region of the MOSFET. As evident from equation (6), the temperature sensitivity of the time span $t_{12}$ is dependent on the transconductance gain $K_n$. An increasing gain corresponds to a steeper current rise and thus to a shortened second time period $t_{12}$.

The temperature dependency of the gain $K_n$ is due to the carrier mobility $\mu_n$ which is evident from equation (5). This is the decisive difference for the sensitivity of the considered TSEP between Si and SiC components since the temperature dependency of the carrier mobility varies greatly for different semiconductor materials. This is in contrast to the temperature dependency of the gate resistance and the threshold voltage, which are similar for both Si and SiC devices.

In Fig. 3, the carrier mobility $\mu_n$ is plotted over junction temperature for a Si device in blue and for a 4H-SiC device in red. The data points of the figure are extracted from publication [29] for the Si component and from publication [30] for the 4H-SiC component. As can be seen in Fig. 3, the carrier mobility decreases with temperature for the Si device and increases with temperature for the SiC device. As a result, for Si devices the carrier mobility

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**Figure 3.** Carrier mobility $\mu_n$ over temperature for Si [29] and 4H-SiC ($\mu_n = 1.4 \times 10^{12} \text{ cm}^2/\text{V} \cdot \text{s}$) [30] devices.
\( \mu_n \), respectively the transconductance gain \( K_n \), has a lengthening influence on the time delay with increasing temperature, whereas it has a shortening influence for SiC components. However, it must be taken into account that, depending on the SiC device, the carrier mobility does not increase indefinitely over temperature. Depending on the structure, e.g., 4H-SiC and 6H-SiC [29], and the free electron concentration in the channel \( n_s \) [30], the carrier mobility begins to decrease over temperature starting with temperatures in the range of 100°C to 220°C. In this higher temperature range, the temperature dependency of the SiC carrier mobility starts to behave similarly to the one of Si devices. Nevertheless, in most cases the assumption of increasing mobility over temperature is correct for a very wide operating range of SiC devices.

The temperature dependency of both the threshold voltage \( U_{th} \) and the transconductance gain \( K_n \) predominantly influences the time periods \( t_{01} \) and \( t_{12} \). For time period \( t_{01} \), this means that the shortening effect of the threshold voltage outweighs the lengthening effect of the gate resistance, resulting in a negative temperature coefficient for this time period. This negative temperature coefficient of time period \( t_{01} \) applies to both Si and SiC devices. In contrast to this, the temperature coefficient of time period \( t_{12} \) differs fundamentally for Si and SiC devices due to the previously described difference in temperature dependency of the transconductance gain. For Si devices, the lengthening influence of the transconductance gain and the gate resistance on the time period \( t_{12} \) outweighs the shortening influence of the threshold voltage, which results in a positive temperature coefficient of this time period. However for SiC devices, the dominant transconductance gain and the threshold voltage both have a shortening influence on time period \( t_{12} \), which results in an overall negative temperature coefficient.

Since for Si components the temperature coefficients of time periods \( t_{01} \) and \( t_{12} \) are different, the temperature sensitivity of the entire time period \( t_{02} \) is reduced. Depending on the Si device and the selection of the trigger level of the inductance voltage \( U_{S',lev} \), this circumstance can, in the worst case, lead to the TSEP exhibiting no temperature sensitivity at all. In contrast, the negative temperature coefficients of both time periods \( t_{01} \) and \( t_{12} \) for SiC devices do not lead to a reduction of the temperature sensitivity of the TSEP. The proposed junction-temperature sensing method is therefore particularly suitable for the application on SiC components.

It is expected that degradation of the power module during operation will impact the parameters that influence the considered TSEP. This means that the time period \( t_{02} \) for a given temperature will change as the power module degrades. Therefore, the accuracy of the junction-temperature sensing method will worsen during operation if the degradation influence is not considered. One aging effect that will have an impact on the TSEP is gate-oxide degradation that is known to decrease the threshold voltage [31].

### 4 Experimental Results

To validate this sensing method, a SiC MOSFET power module by Cree (CAS120M12BM2) [32] has been tested on a double-pulse test bench [33] for a dc-link voltage of \( U_{dc} = 700 \) V. The module was heated to the desired temperature by using a peltier-based thermal control unit [34]. The MOSFET was switched using a gate driver with a turn-on voltage \( U_{D, on} = 20 \) V, a turn-off voltage \( U_{D, off} = -5 \) V and an external gate resistance of \( R_{G, ext} = 3.3 \) Ω. The gate voltage \( u_{GS,m} \) was measured using a Testec TT-SI9101 voltage probe while the voltage \( u_{LS} \) across the parasitic inductance was acquired using

![Figure 4. Double-pulse test bench with SiC power module attached to a peltier-based temperature-control unit, gate driver and test equipment to extract the gate voltage \( u_{GS,m} \) and the parasitic-inductance voltage \( u_{LS} \) during turn-on process.](image)

![Figure 5. Measured gate driver voltage \( u_{GS,m} \) and parasitic-inductance voltage \( u_{LS} \) for three junction temperatures (30 °C, 70 °C, 110 °C) and a device current \( I_{DS} = 110 \) A during the turn-on process of a SiC MOSFET.](image)
a PMK BumbleBee voltage probe. The measurement data was captured with a LeCroy Teledyne HDO 6104 oscilloscope. The double-pulse test bench with the device under test (DUT) attached to the temperature-control unit, the gate driver and the test equipment can be seen in Figure 4.

Figure 5 shows the measured gate voltage $u_{GS,m}$ and the parasitic-inductance voltage $u_{S'S}$ for three different junction temperatures and for a device current $i_{DS} = 110 \, \text{A}$ during the turn-on process of the SiC MOSFET. The time instant $t = 0 \, \text{ns}$, at which the gate voltage $u_{GS,m}$ begins to rise, corresponds to the beginning of time period $t_{01}$. This time period ends with the beginning of the rise of the parasitic-inductance voltage $u_{S'S}$ that occurs at around 28 ns in this case. It is evident that the rise of the inductance voltage $u_{S'S}$ starts slightly earlier for higher temperatures, which shortens time period $t_{01}$. This behavior confirms the previous assumption of a negative temperature coefficient of this first time period due to the dominant influence of the threshold voltage $U_{th}$. Time period $t_{12}$ starts with the rise of the parasitic-inductance voltage $u_{S'S}$ and ends when this voltage reaches a defined trigger level $U_{S'S,lev}$. It can be seen that the voltage rise $\frac{du_{S'S}}{dt}$ becomes steeper for higher temperatures, resulting in a shorter time period $t_{12}$. This confirms the assumption of an increasing transconductance gain $K_m$ with temperature and a negative temperature coefficient of time period $t_{12}$ for SiC MOSFETs. The negative temperature coefficient of both time periods $t_{01}$ and $t_{12}$ confirms the particular suitability of the measurement method for SiC MOSFETs.

Figure 6 shows the measured gate voltage $u_{GS,m}$ and the parasitic-inductance voltage $u_{S'S}$ during the turn-on process of the SiC MOSFET for three device currents (70 A, 90 A, 110 A) and a junction temperature of 30 °C. It is evident that the progressions of the parasitic-inductance voltage $u_{S'S}$ for different device currents show a very similar behavior. This confirms the previous assumption of a low device-current sensitivity of the considered TSEP that allows a minimal calibration effort of the junction-temperature sensing method.

The time delay $t_{02}$ extracted from measurements for a voltage trigger level $U_{S'S,lev} = 37 \, \text{V}$ is shown in Figure 7. The delay is plotted over a temperature range from 30 °C to 110 °C and for three device currents (70 A, 90 A, 110 A). On the one hand, these results once again confirm the low device-current sensitivity of the time delay, since the curves for the three different device currents are well superimposed. On the other hand, an approximately linear course of the time delay can be observed that, in addition to the low current sensitivity, can reduce the calibration effort up to a 2-point measurement.

From the results in Figure 7, a resolution of the time delay of about 30 ps can be derived. To extract the time delay during operation, commercial time-to-digital converter integrated circuits (ICs) can be used. When using a time-to-digital IC, no analog-to-digital converter (ADC) is required. Thus, the junction-temperature sensing method represents a more cost-effective alternative to other TSEP extraction methods requiring high performance ADCs. One example for a time-to-digital IC is the widely available and inexpensive Texas Instrument TDC7200, which has a theoretical time resolution of 50ps.

### 5 Conclusions

The key conclusions of this work can be summarized as follows: The extraction of the turn-on delay as a high-bandwidth junction-temperature sensing method is particularly suitable for applying to SiC MOSFETs. In comparison to Si devices, the positive temperature coefficient of the charge carrier mobility for SiC components has a favorable influence on the temperature sensitivity of the TSEP. Furthermore, the low device-current sensitivity
and the linear temperature dependency of the delay allow a low calibration effort up to a 2-point measurement. The use of a time-to-digital IC for the extraction of the time delay offers the potential for a more cost-effective alternative than TSEP extraction methods that rely on a high-performance ADC. The junction-temperature sensing method was evaluated on an SiC power module using a double-pulse test bench with temperature-control unit.

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